

TITLE 800G OSFP-IHS Active Electrical Cable - PAM4	DOC No. RFD-20260304601-001	
	REVISION : 01	AUTHORIZED BY : Jeff Lo
	DATE : 2026.03.04	CLASSIFICATION : Active Electrical Cable

1. PRODUCT FEATURES

- Compliant with IEEE 802.3ck and OSFP MSA
- Compliant with CMIS5.2
- Support 8x112G (PAM4) electrical data rates
- Enables 800Gb/s transmission
- Selectable: 26AWG, 28AWG, 30AWG, 32AWG
- Link Length up to 7m
- Typical power consumption 12W per end
- Single +3.3V power supply
- BER (Post-FEC) <10⁻¹⁵
- Operation case temperature: 0 to 70°C
- RoHS compliant

2. APPLICATION

- Data Centre
- Router, Server, Storage, Switch

3. ABSOLUTE MAXIMUM RATINGS

Parameter	Unit	Min.	Typical	Max.	Notes
Storage Temperature	°C	-45		80	
Operating Relative Humidity	%			85	
Power Supply not Damaged Voltage	V	-0.5		3.6	

4. RECOMMENDED OPERATING CONDITIONS

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Parameter	Unit	Min.	Typical	Max.	Notes
Operating Case Temperature	°C	0		70	
Power Supply Working Voltage	V	3.135	3.3	3.465	
Bit Rate	Gbps		800		

5. PIN FUNCTION DEFINITIONS

Pin#	Symbol	Description	Logic	Direction	Plug Sequence	Notes
1	GND	Ground			1	
2	TX2p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
3	TX2n	Transmitter Data Inverted	CML-I	Input from Host	3	
4	GND	Ground			1	
5	TX4p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
6	TX4n	Transmitter Data Inverted	CML-I	Input from Host	3	
7	GND	Ground			1	
8	TX6p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
9	TX6n	Transmitter Data Inverted	CML-I	Input from Host	3	
10	GND	Ground			1	
11	TX8p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
12	TX8n	Transmitter Data	CML-I	Input from Host	3	

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		Inverted				
13	GND	Ground			1	
14	SCL	2-wire Serial interface clock	LVCMO S-I/O	Bi-directional	3	Open-Drain with pull- up resistor on Host
15	VCC	+3.3V Power		Power from Host	2	
16	VCC	+3.3V Power		Power from Host	2	
17	LPWn/P RSn	Low-Power Mode / Module Present	Multi-Le vel	Bi-directional	3	See pin description for required circuit
18	GND	Ground			1	
19	RX7n	Receiver Data Inverted	CML-O	Output to Host	3	
20	RX7p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
21	GND	Ground			1	
22	RX5n	Receiver Data Inverted	CML-O	Output to Host	3	
23	RX5p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
24	GND	Ground			1	
25	RX3n	Receiver Data Inverted	CML-O	Output to Host	3	
26	RX3p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
27	GND	Ground			1	
28	RX1n	Receiver Data Inverted	CML-O	Output to Host	3	
29	RX1p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
30	GND	Ground			1	
31	GND	Ground			1	

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32	RX2p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
33	RX2n	Receiver Data Inverted	CML-O	Output to Host	3	
34	GND	Ground			1	
35	RX4p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
36	RX4n	Receiver Data Inverted	CML-O	Output to Host	3	
37	GND	Ground			1	
38	RX6p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
39	RX6n	Receiver Data Inverted	CML-O	Output to Host	3	
40	GND	Ground			1	
41	RX8p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
42	RX8n	Receiver Data Inverted	CML-O	Output to Host	3	
43	GND	Ground			1	
44	INT/RS Tn	Module Interrupt / Module Reset	Multi-Level	Bi-directional	3	See pin description for required circuit
45	VCC	+3.3V Power		Power from Host	2	
46	VCC	+3.3V Power		Power from Host	2	
47	SDA	2-wire Serial interface data	LVCMOS-I/O	Bi-directional	3	Open-Drain with pull-up resistor on Host
48	GND	Ground			1	
49	TX7n	Transmitter Data Inverted	CML-I	Input from Host	3	
50	TX7p	Transmitter Data	CML-I	Input from Host	3	

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		Non-Inverted				
51	GND	Ground			1	
52	TX5n	Transmitter Data Inverted	CML-I	Input from Host	3	
53	TX5p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
54	GND	Ground			1	
55	TX3n	Transmitter Data Inverted	CML-I	Input from Host	3	
56	TX3p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
57	GND	Ground			1	
58	TX1n	Transmitter Data Inverted	CML-I	Input from Host	3	
59	TX1p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
60	GND	Ground			1	

6. ELECTRICAL PAD LAYOUT

For detail mechanical information, please refer to the related document of OSFP MSA.

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Top Side (viewed from top)

60	GND	
59	TX1p	
58	TX1n	
57	GND	
56	TX3p	
55	TX3n	
54	GND	
53	TX5p	
52	TX5n	
51	GND	
50	TX7p	
49	TX7n	
48	GND	
47	SDA	
46	VCC	
45	VCC	
44	INT/RSTn	
43	GND	
42	RX8n	
41	RX8p	
40	GND	
39	RX6n	
38	RX6p	
37	GND	
36	RX4n	
35	RX4p	
34	GND	
33	RX2n	
32	RX2p	
31	GND	

Module Card Edge

Bottom Side (viewed from bottom)

	GND	1
	TX2p	2
	TX2n	3
	GND	4
	TX4p	5
	TX4n	6
	GND	7
	TX6p	8
	TX6n	9
	GND	10
	TX8p	11
	TX8n	12
	GND	13
	SCL	14
	VCC	15
	VCC	16
	LPWn/PRSn	17
	GND	18
	RX7n	19
	RX7p	20
	GND	21
	RX5n	22
	RX5p	23
	GND	24
	RX3n	25
	RX3p	26
	GND	27
	RX1n	28
	RX1p	29
	GND	30

7. MECHANICAL OUTLINES

7.1 Product Name And Series Number(s)

800G OSFP Active Electrical Cable - PAM4

JPC P/N	Length(m)	Cable AWG	Description
P83**7W0a**M-1	0.25m – 3.0m	30 AWG	800G OSFP AEC PAM4 30AWG **m
P83**7Y0a**M-1	3.25m – 7.0m	26 AWG	800G OSFP AEC PAM4 26AWG **m

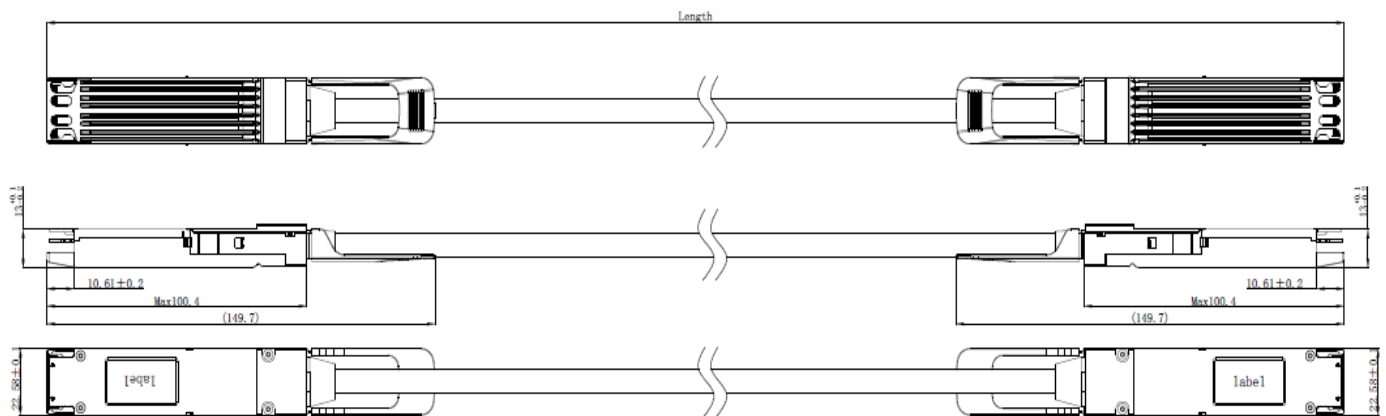
Note-1 : ** Indicates the customer code.

Note-2 : a Indicates the Housing Heat Sink

e.g. A means IHS-IHS, B means RHS-RHS, C means IHS-RHS

Note-3 : ** Indicates the length.

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Unit:mm

IHS to IHS Mechanical Dimensions

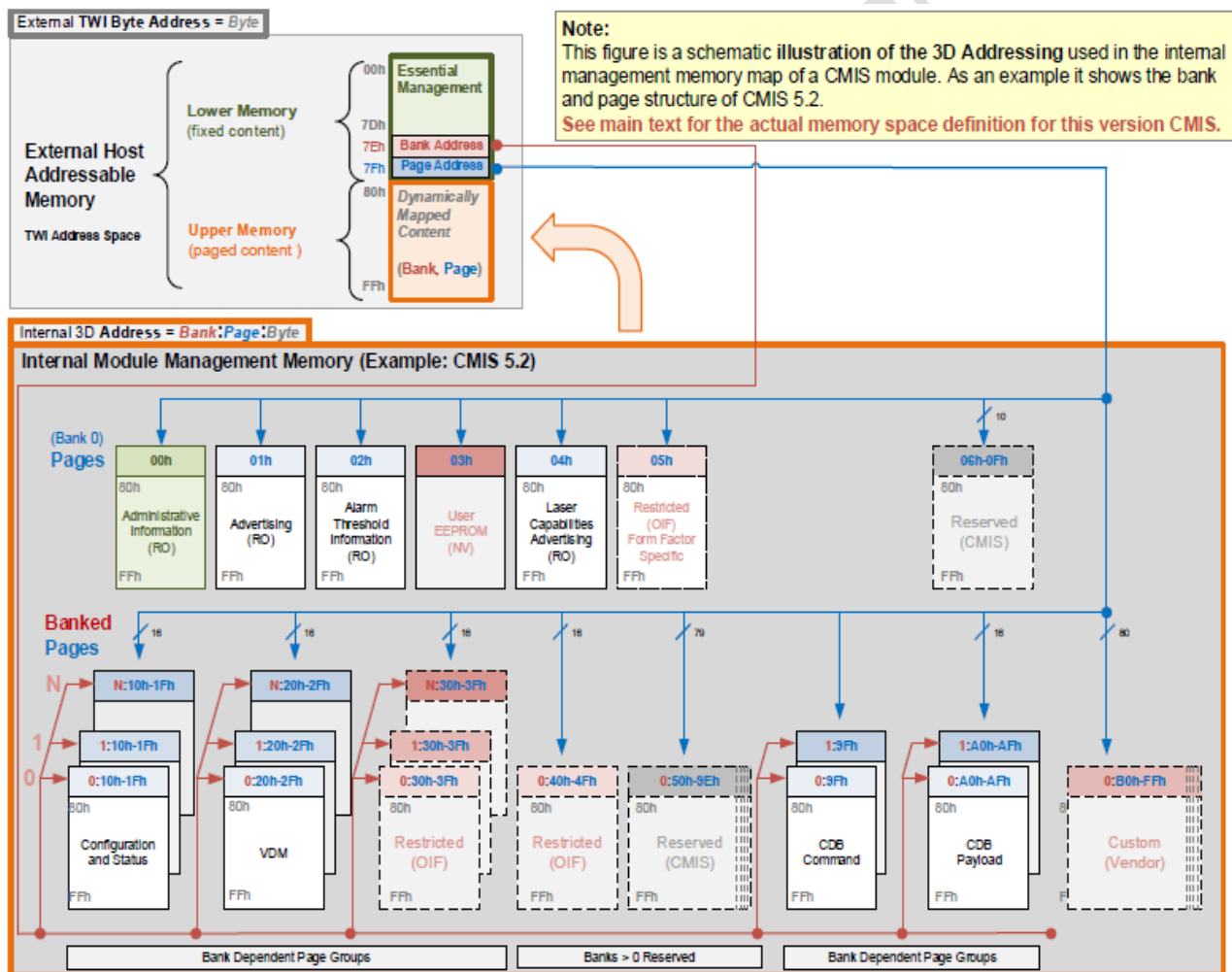
Length (m)	Cable AWG
0.25m – 3.0m	30
3.25m – 7.0m	26

8. EEPROM INFORMATION

The digital diagnostic memory map specific data field defined as following. For detail EEPROM information, please refer to the related document of CMIS5.2.

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9. Modification History

Rev.	Comments	Date	Originator	Approval
01	Preliminary Draft	2026.03.04	Jeff Lo	Mike Sun